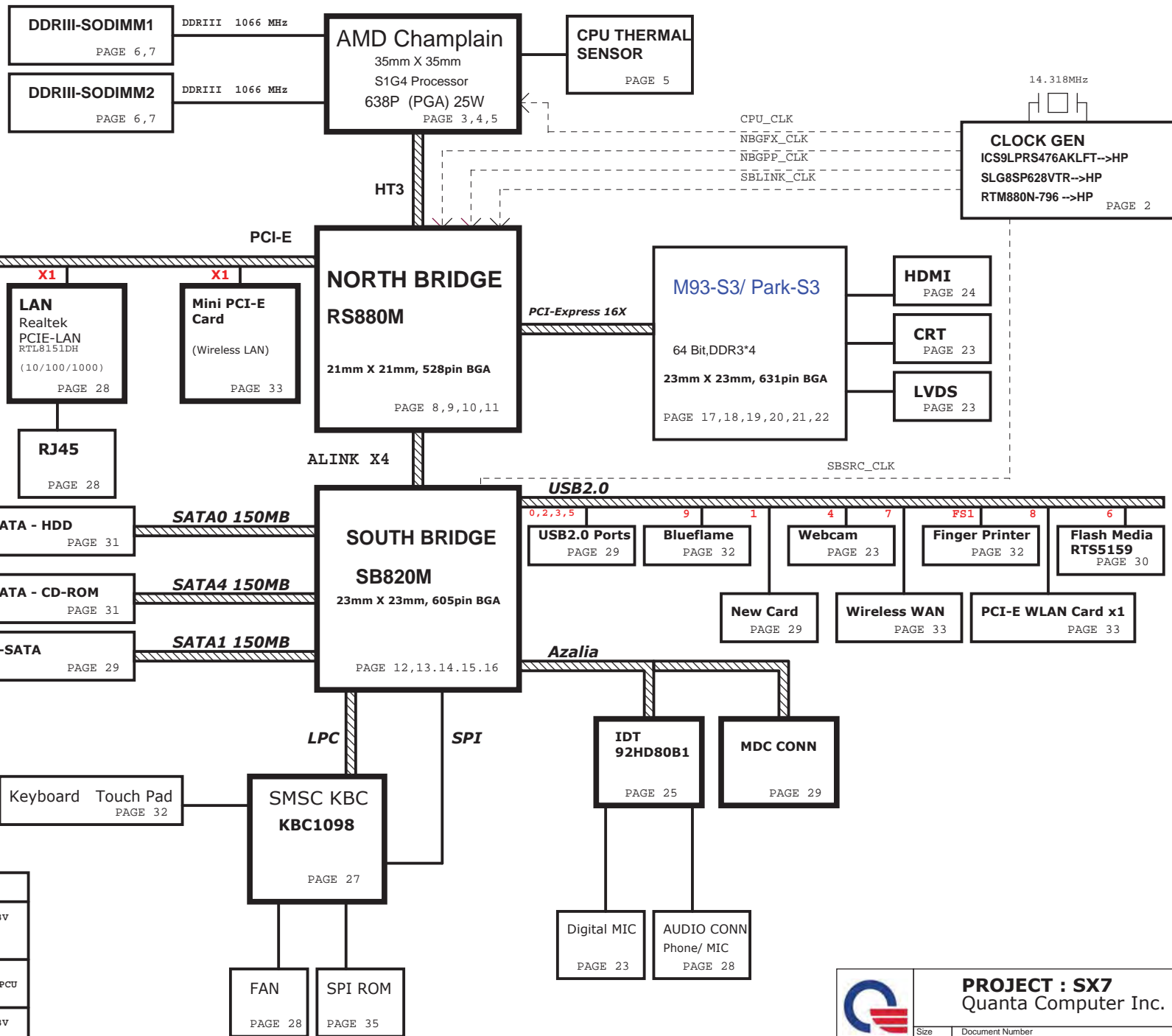
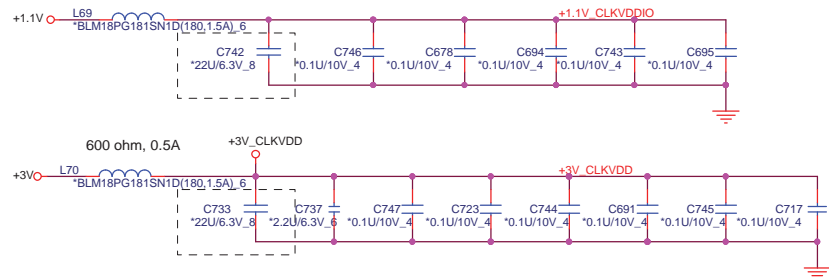


PCB STACK UP

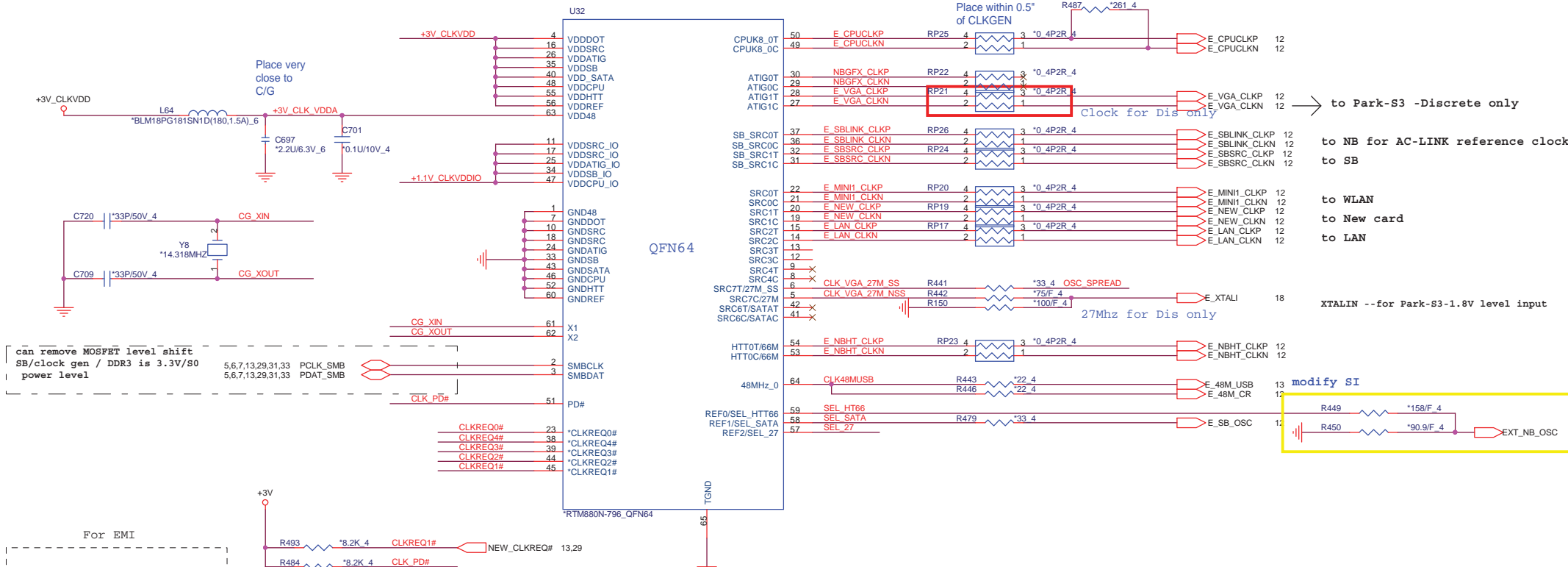
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT





CLOCKS name	Discrete	Clock pin function
NBGF_X_CLKP NBGF_X_CLKN	NA	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP21 STUFF	to Park-S3 external reference clock -Discrete only
SBLINK_CLKP SBLINK_CLKN	RP26 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R441, R442 STUFF	To Park-S3 27Mhz - Discrete only

Need check the net name for the short pad



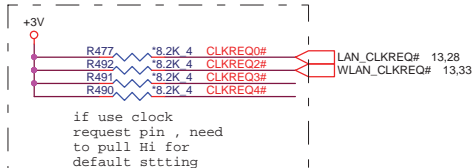
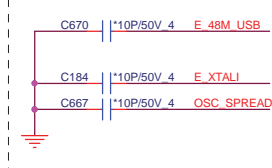
can remove MOSFET level shift
SB/clock gen / DDR3 is 3.3V/S0
power level

5,6,7,13,29,31,33 PCLK_SMB
5,6,7,13,29,31,33 PDAT_SMB

CLK_PD#

CLKREQ0# 23
CLKREQ4# 38
CLKREQ3# 39
CLKREQ2# 44
CLKREQ1# 45
*CLKREQ0#
*CLKREQ4#
*CLKREQ3#
*CLKREQ2#
*CLKREQ1#

For EMI

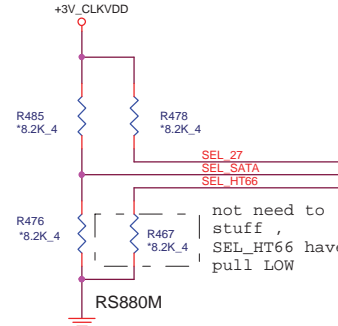


if use clock
request pin, need
to pull Hi for
default stting

IDT ICS9LPRS480AKLFT--ALPRS480000
SLG SLG8SP628VTR--AL8SP628000
RTL RTM880N-796-- AL000880001

* default

SEL_HT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

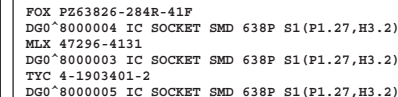


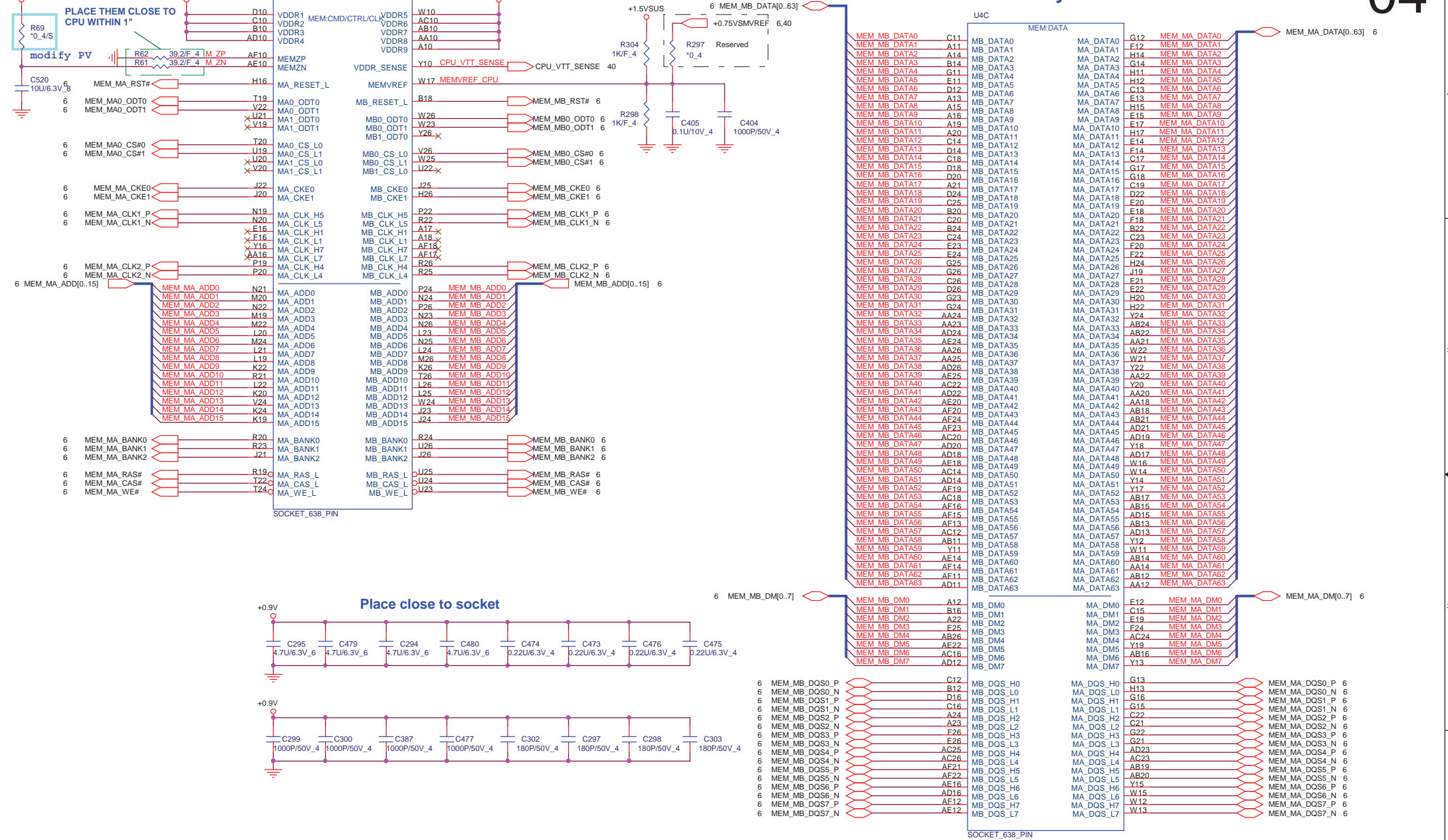
Clock chip has internal serial
terminations
for differential pairs, external resistors
are
reserved for debug purpose.

PROJECT : SX7
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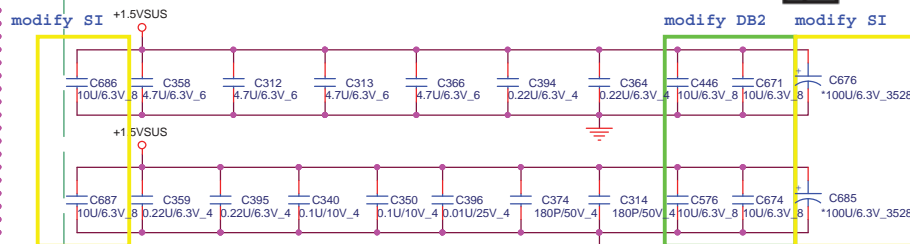
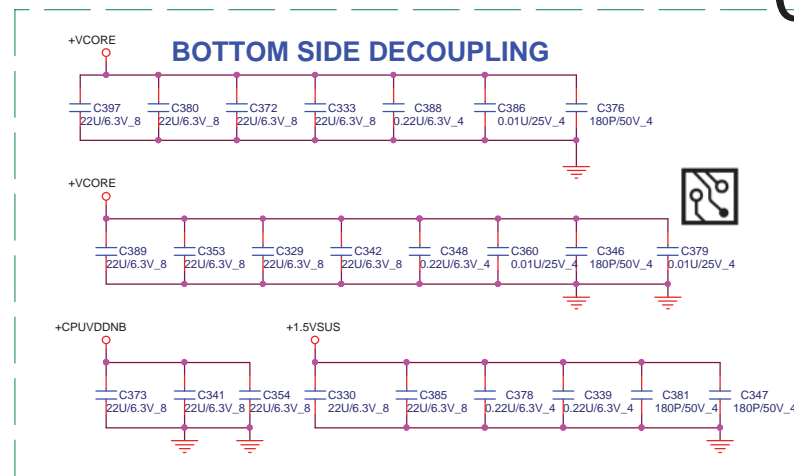
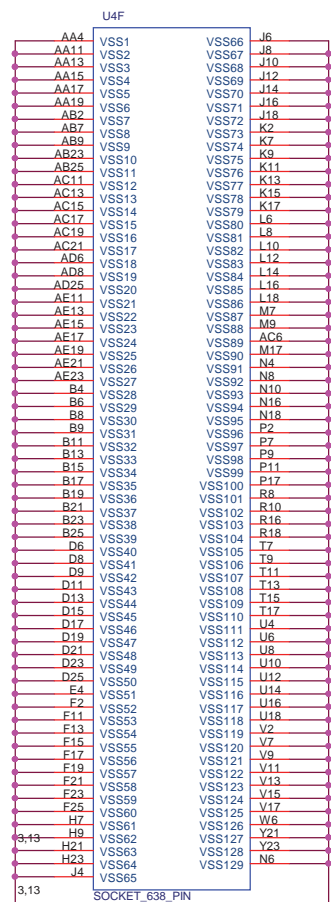
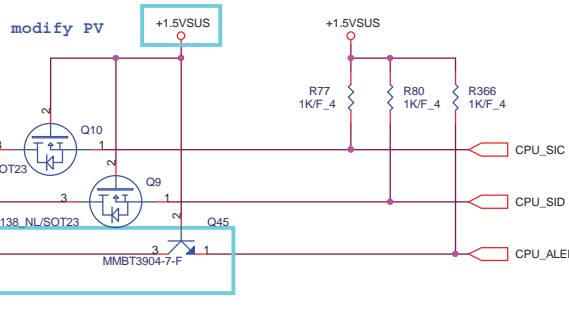
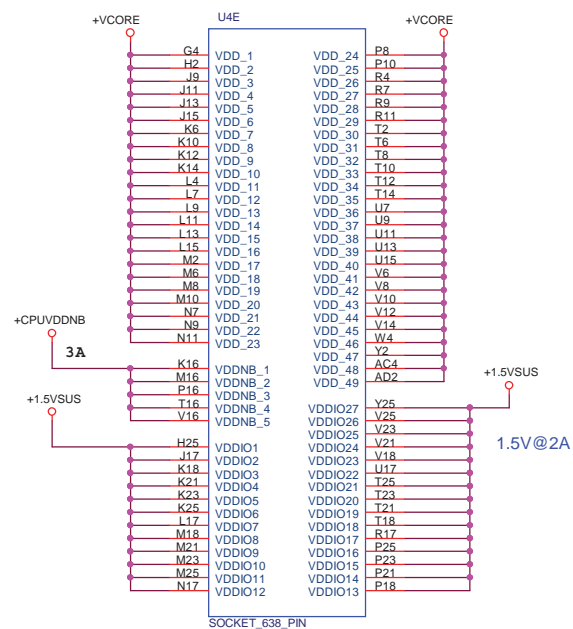
Size Custom Document Number Clock Generator Rev 3A

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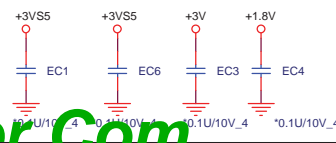
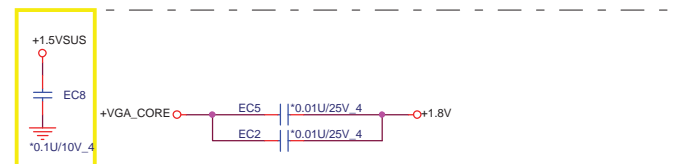


3.5,6,7,40,41,42 +1.5VSUS
6,40 +0.75VSMVREF
41 +0.9V



PROCESSOR POWER AND GROUND

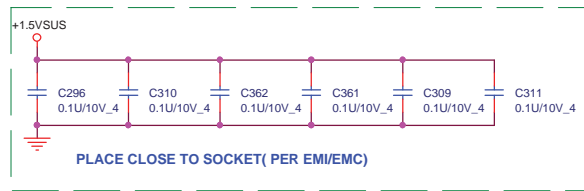
For fix HyperTransport nets
across plane splits



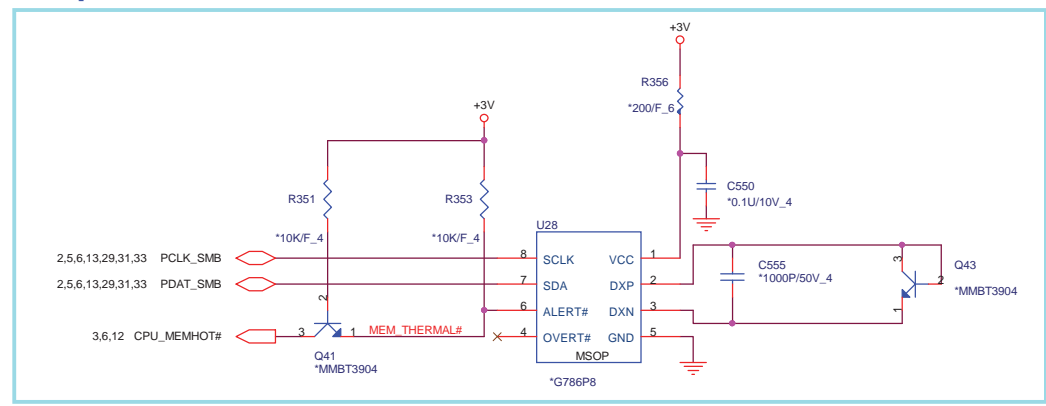
PROJECT : SX7
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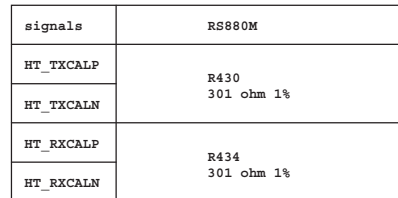
Size Custom	Document Number S1G2 PWR & GND 3/3	R
Date: Monday, March 15, 2010	Sheet 5 of 43	





modify PV





U5D

PAR 4 OF 6

SBD - MEM/DVO_I / F

Pin	Signal	Signal	Signal
AB12	MEM_A0(NC)	MEM_DQ0/DVO_VSYNC(NC)	AA18
AE16	MEM_A1(NC)	MEM_DQ1/DVO_HSYNC(NC)	AA20
X V11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)	AA19
AE15	MEM_A3(NC)	MEM_DQ3/DVO_D0(NC)	Y19
AA12	MEM_A4(NC)	MEM_DQ4(NC)	Y17
AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)	AA17
AB14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)	AA15
AD14	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)	Y15
AD13	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)	AC20
AD16	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)	AD19
AC16	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)	AE22
AE13	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)	AC18
AC14	MEM_A12(NC)	MEM_DQ12(NC)	AB20
X Y14	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)	AD22
		MEM_DQ14/DVO_D10(NC)	AC22
AD16	MEM_BA0(NC)	MEM_DQ15/DVO_D11(NC)	AD21
AE17	MEM_BA1(NC)		
AD17	MEM_BA2(NC)	MEM_DQS0P/DVO_IDCKP(NC)	Y17
		MEM_DQS0N/DVO_IDCKN(NC)	W18
X W12	MEM_RASb(NC)	MEM_DQS1P(NC)	AD20
X Y12	MEM_CASb(NC)	MEM_DQS1N(NC)	AE21
AD18	MEM_WEb(NC)		
AB13	MEM_CSb(NC)	MEM_DM0(NC)	W17
AB18	MEM_CKE(NC)	MEM_DM1/DVO_D8(NC)	AE19
X V14	MEM_ODT(NC)		
X V15	MEM_CKP(NC)	IOPLLVD18(NC)	AE23
X W14	MEM_CKN(NC)	IOPLLVD0(NC)	AE24
		IOPLLVS(NC)	AD23
AE12	MEM_COMPP(NC)		
AD12	MEM_COMPN(NC)	MEM_VREF(NC)	AE18

RS880/RX881

R311
*0_4/S

BLM18PG181SN1D(180,1.5A) 6

BLM18PG181SN1D(180,1.5A) 6

L8

L9

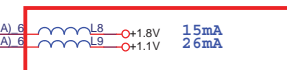
+1.8V

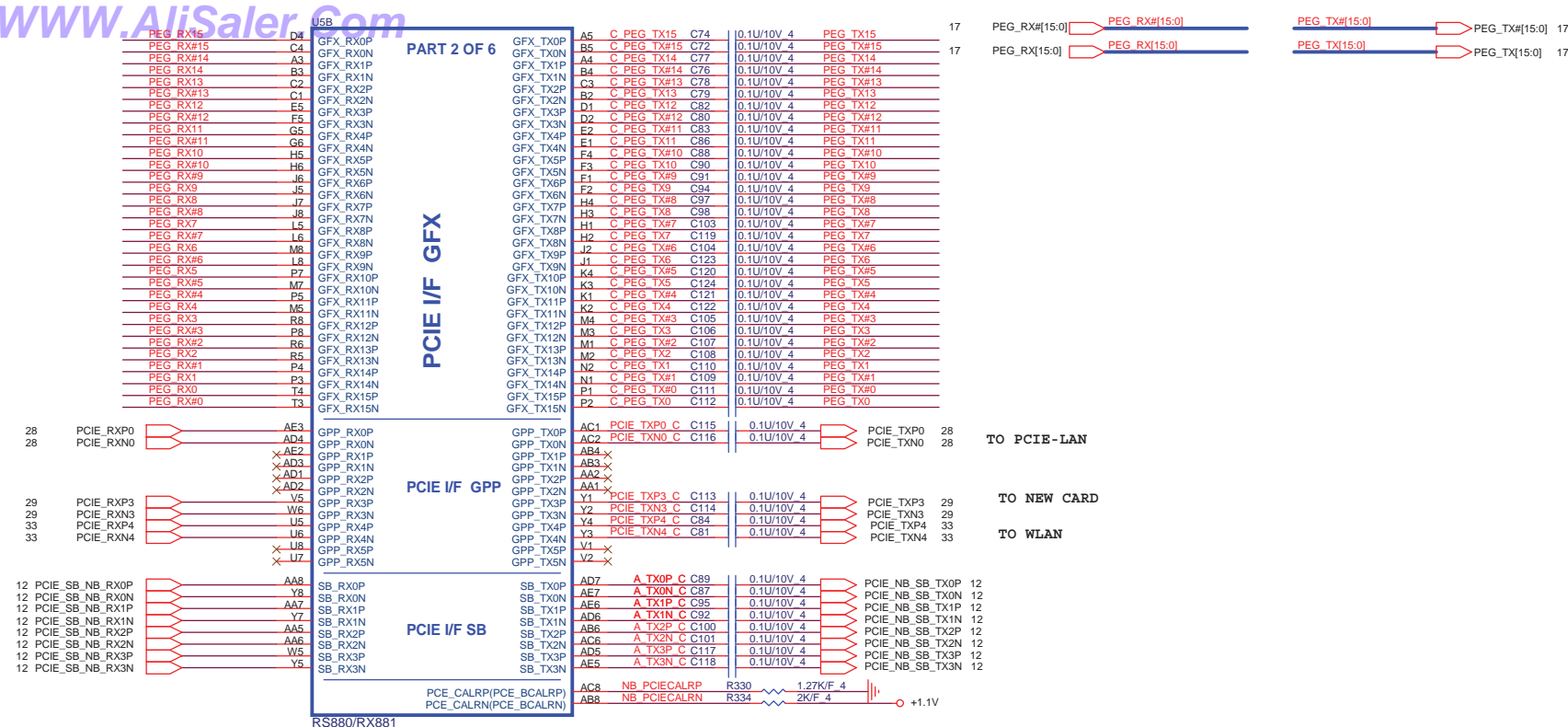
+1.1V

15 mA

26 mA

SPM_VREF1





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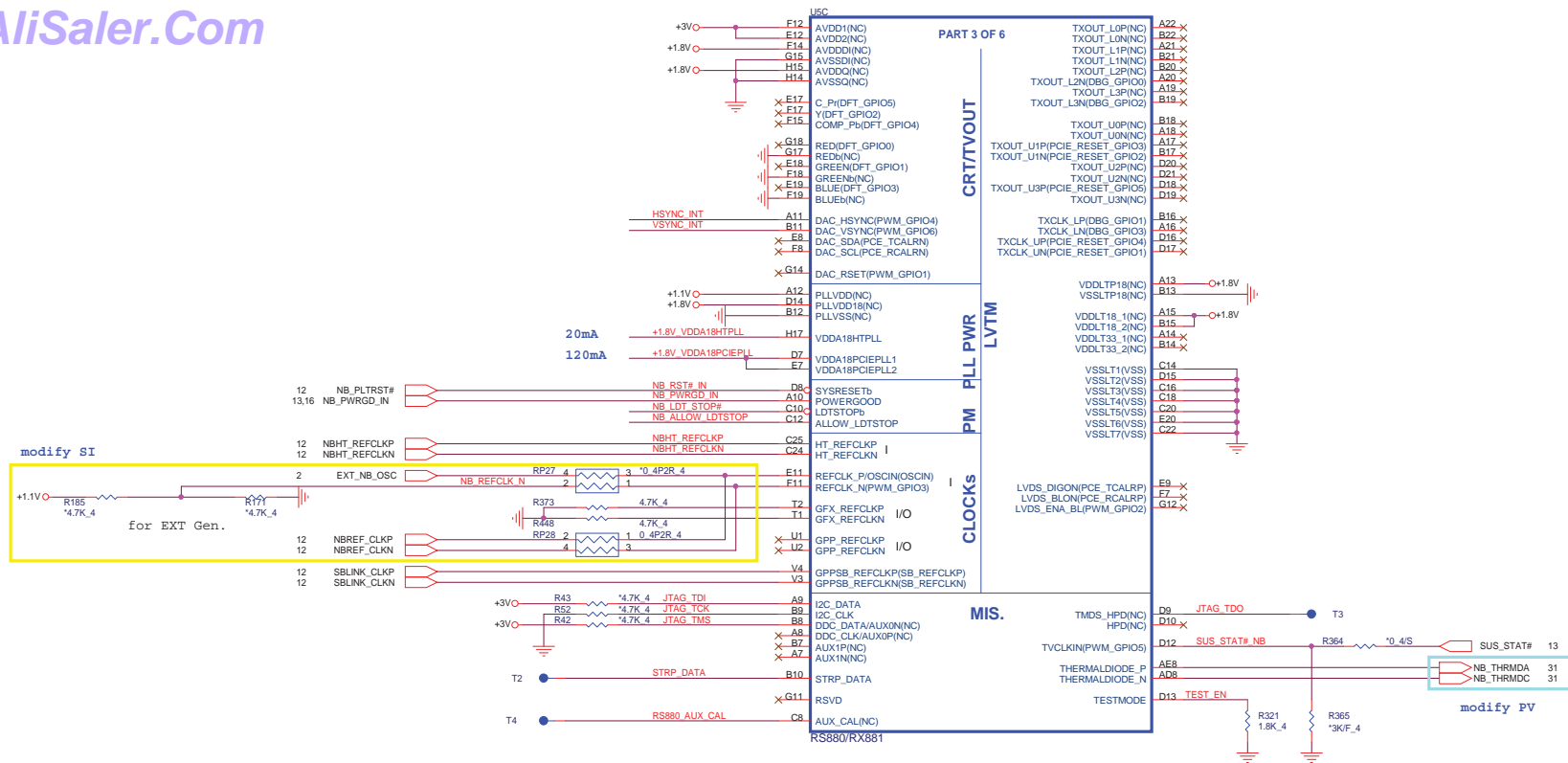
Size
Custom

Document Number
RS880M-PCIE I/F 2/5

Rev
3A

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Discrete

Enables Debug Bus access through memory I/O pads and GPIO.

0 : Enable RS880M , Default

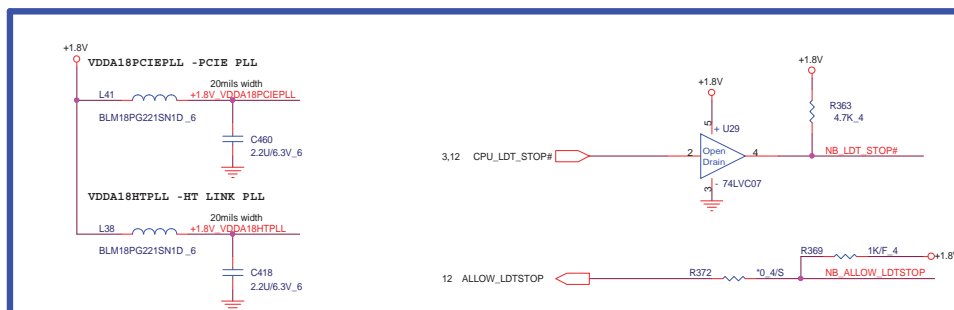
1 : Disable RS880M (RX881 use DAC_VSYNC)

Discrete

Indicates if memory Side port is available or not

0 : Reserved

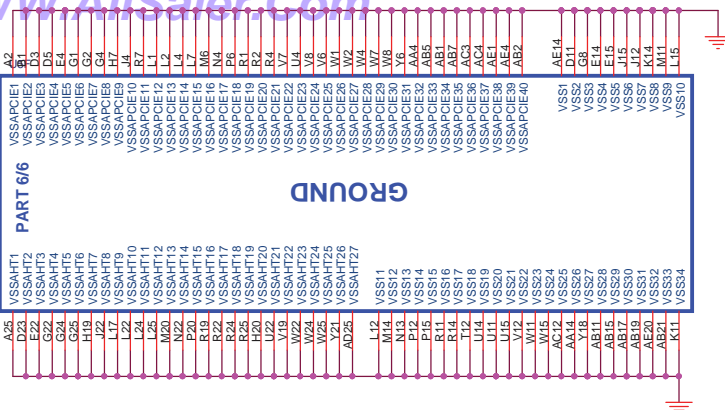
1 : Required setting. Select with a pull-up resistor on the strap (RX881 use DAC_HSYNC)



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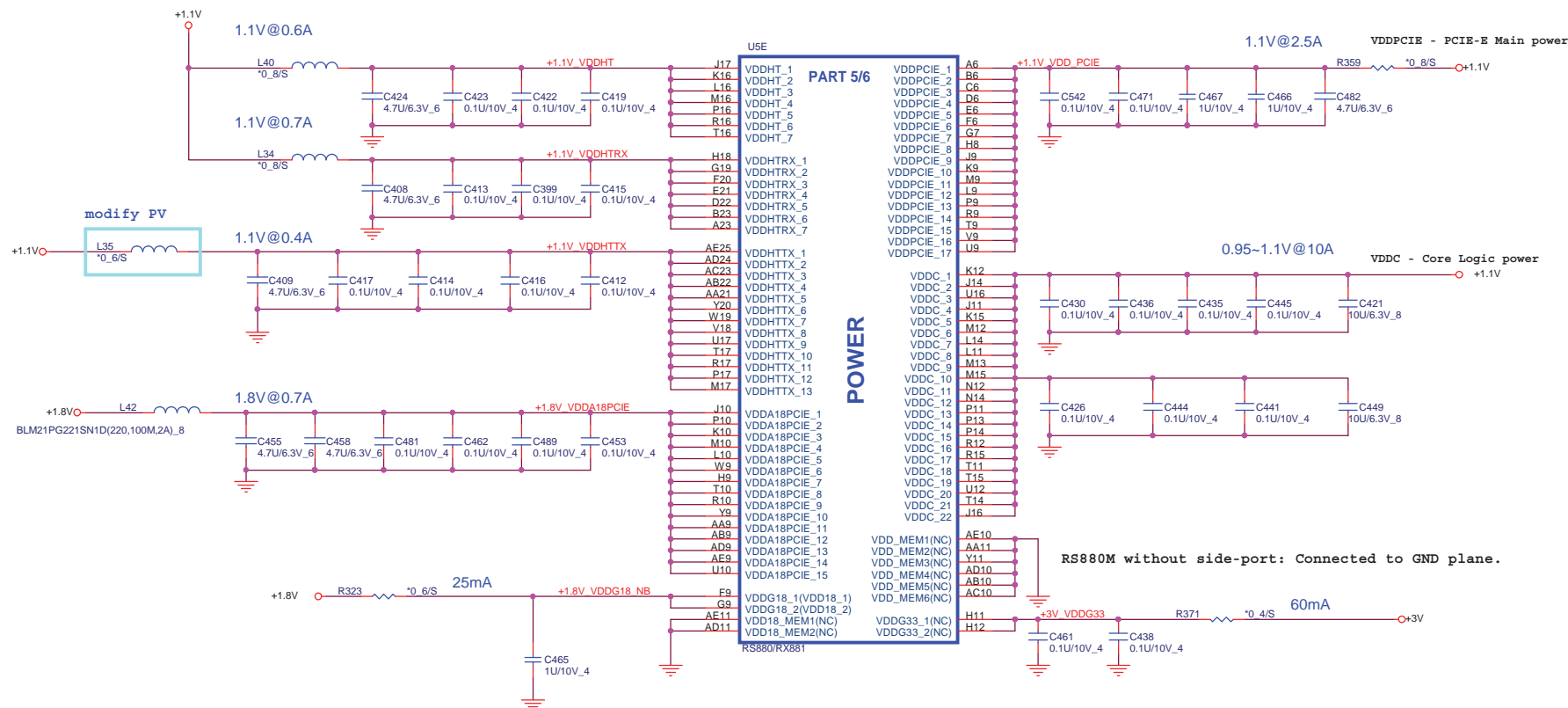
Size Custom Document Number
NB5/RD2 RS880M-SYSTEM I/F 3/5 Rev 3A

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RX881/RS880 POWER DIFFERENCE TABLE

PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	IOPLLVD	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	GND	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDI	GND	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	GND	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	GND	+1.1V
VDD18_MEM	GND	+1.8V	PLLVD18	GND	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	GND	+1.8V/1.5V	VDDLTP18	GND	+1.8V
VDDG33	+3.3V	+3.3V	VDDL18	GND	+1.8V
IOPLLVD18	+1.8V	+1.8V	VDDL33	NC	NC



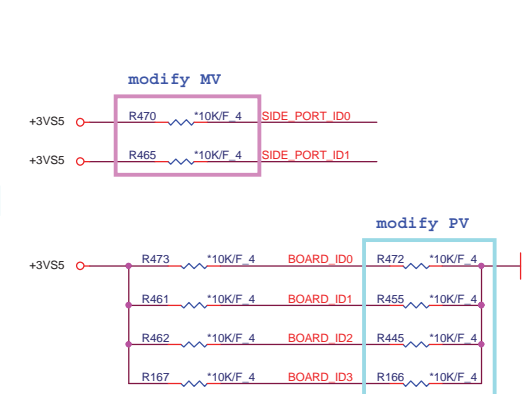
PROJECT : SX7
Quanta Computer Inc.

Size Custom	Document Number RS880M-POWER5/5	Rev 3A
Date: Monday, March 15, 2010	Sheet 11 of 43	



Size Custom	Document Number SB820-PCIE/PCI/CPU/LPC 1/4	Rev 3A
Date: Monday, March 15, 2010		Sheet 12 of 43

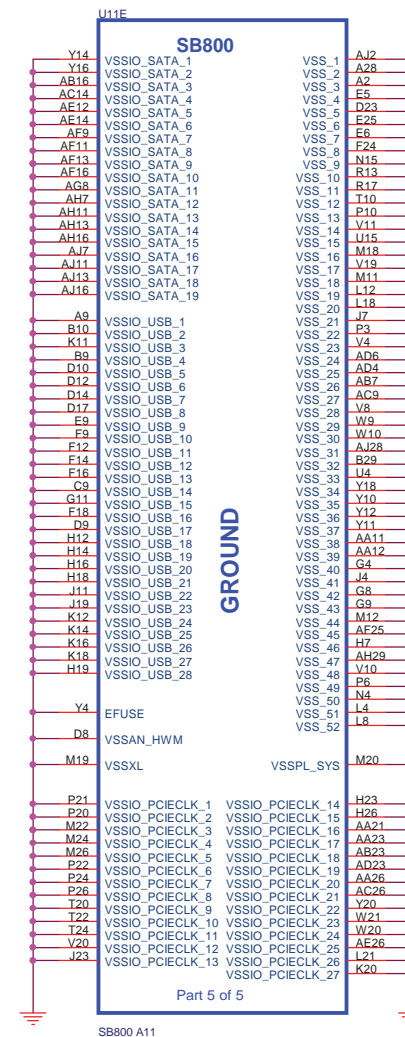


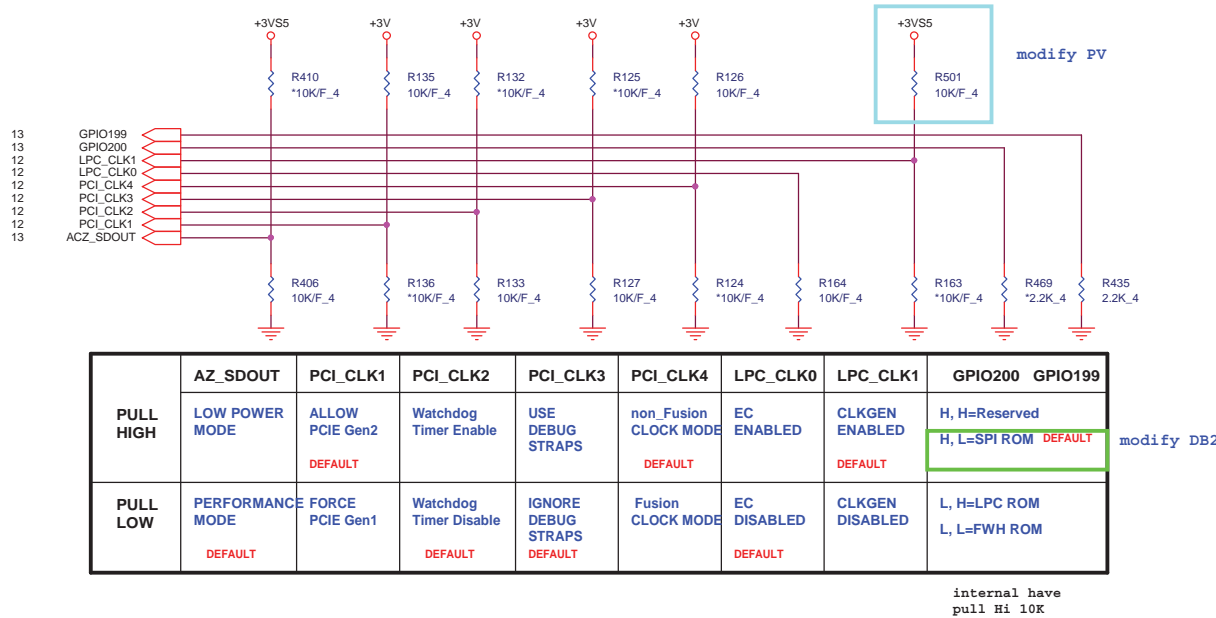


ID3	ID2	ID1	ID0	
0	0	0	0	SX7 UMA
0	0	0	1	SX7 UMA
0	0	1	0	SX7 Dis
0	0	1	1	SX7 Dis
0	1	0	0	SX7 UMA DF
0	1	0	1	SX7 UMA DF
0	1	1	0	SX7 Dis DF
0	1	1	1	SX7 Dis DF



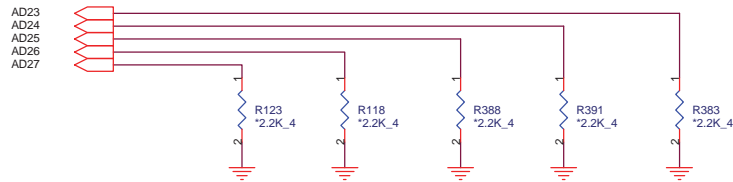
	Re 3
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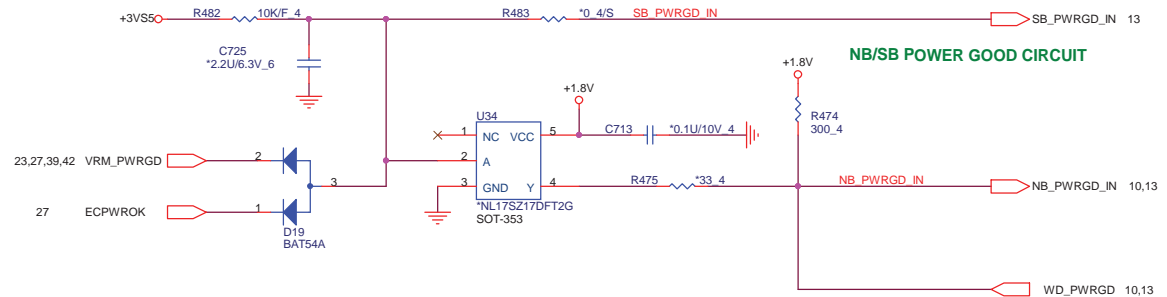


DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

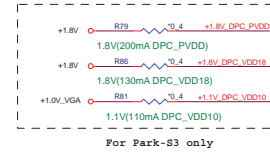
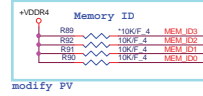


PROJECT : SX7
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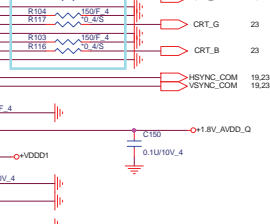
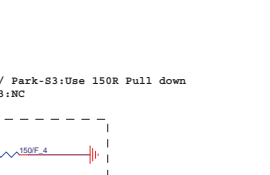
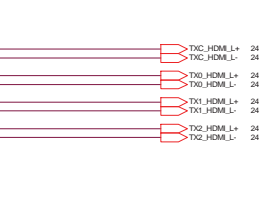
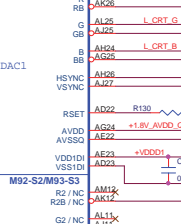
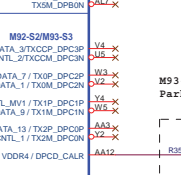
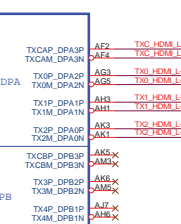
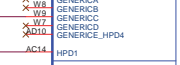
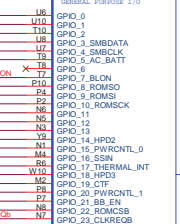
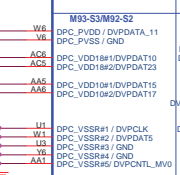
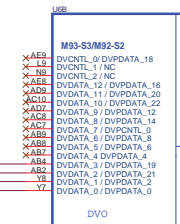
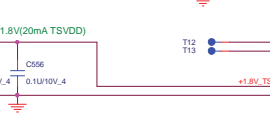
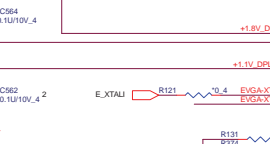
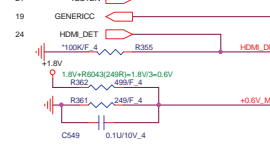
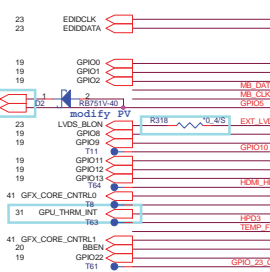
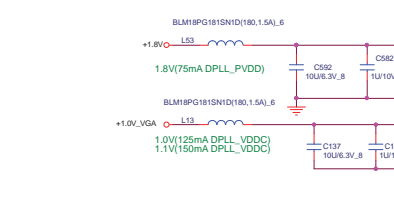
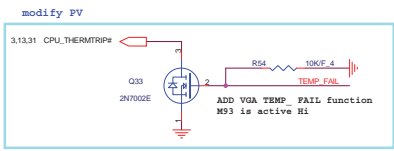
MEM_ID[2:0]	Vendor	Type	Vendor P/N
000	Samsung E-die	54M*16-800MHZ	4W1G1646E-HC12
100	Hynix Orion-die	54M*16-800MHZ	5TQ1G63BFR-12C
010	Samsung E-die	128M*16-800MHZ	
110	Hynix Orion-die	128M*16-800MHZ	

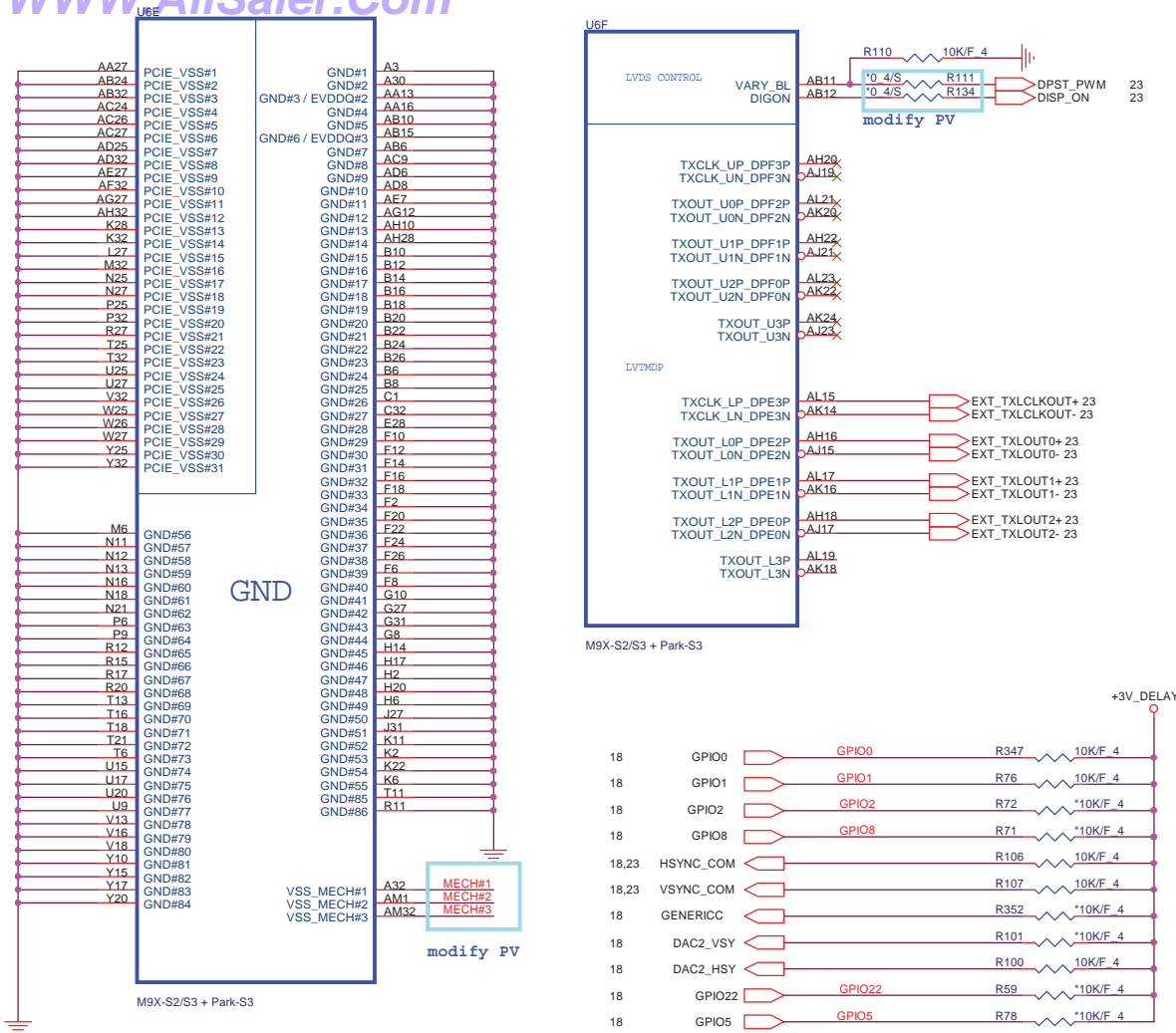


PWRCNTL1	PWRCNTL0	V-CORE
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V

BBEN	BBP
L 0	V-CORE
H 1	+1.8V

No need *CLK_27M_SS* connect to GP10_16, since M9x chip support memory SS function in VBIOS





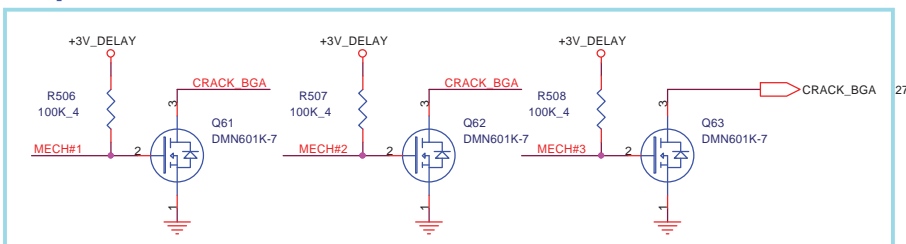
Strap Name	Pin	Straps description	Default Value
TX_PWRS_ENB	GPIO0	PCI Express Full TX Output Swing 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
RSVD	GPIO8	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
BIF_VGA_DIS	GPIO9		0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	1
AUD [0]	VSYNC	AUD[1] AUD[0] 00 No Audio function 01 Audio for DisplayPort and HDMI if #angle is detected 10 Audio for DisplayPort only 11 Audio for both DisplayPort and HDMI	1
AUD (1)	HSYNC		1
VIP_DEVICE_STRAP_ENA	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO.	0
RSVD	GENERICC		0

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

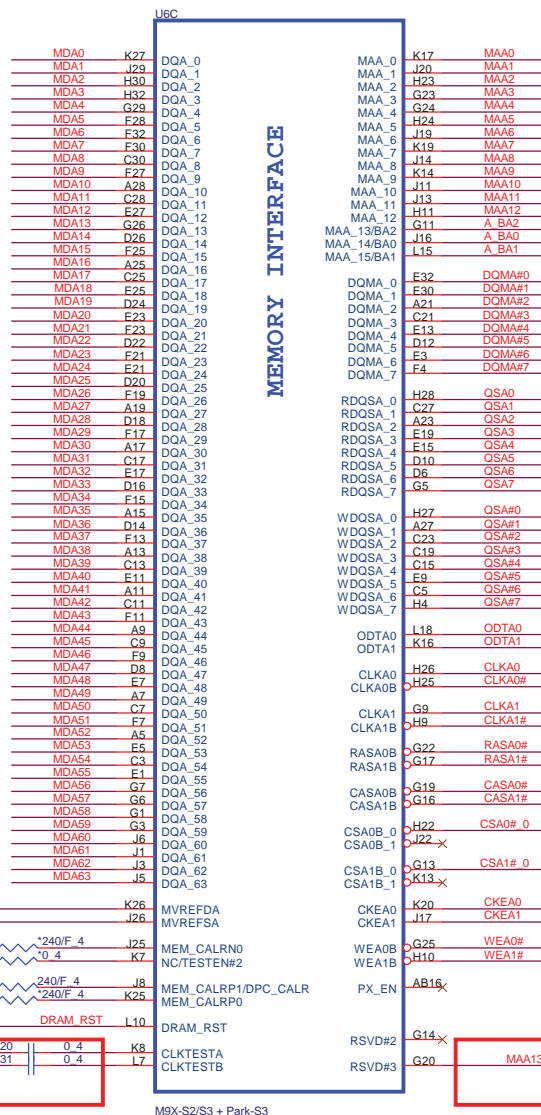
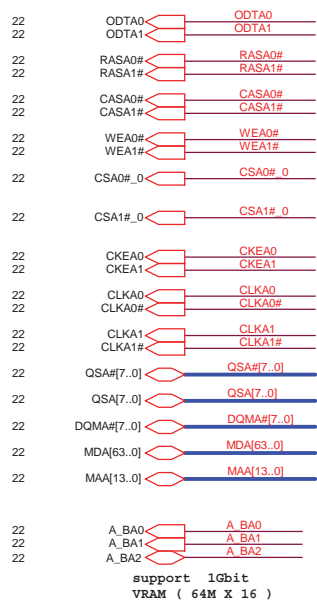
modify PV



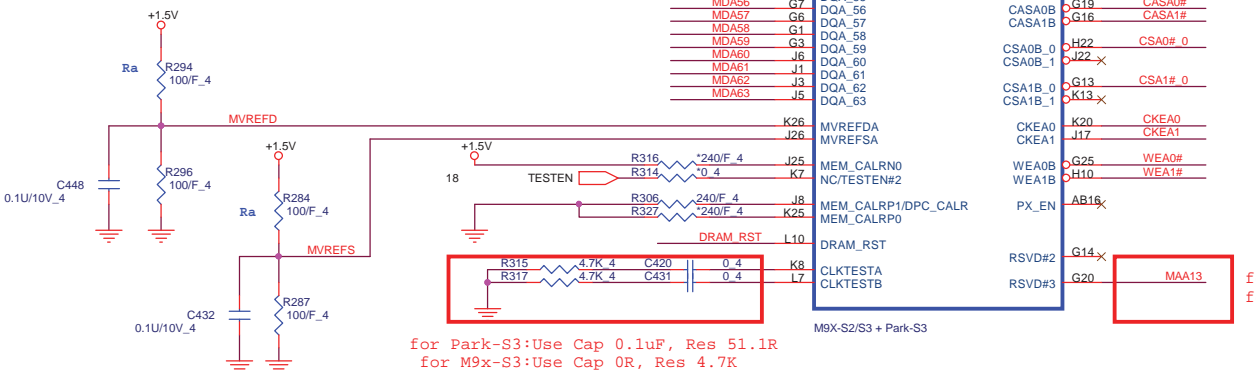
PROJECT : SX7
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Size Custom	Document Number Park_GND / LVDS/ Straps	Rev 3A
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MEMORY INTERFACE

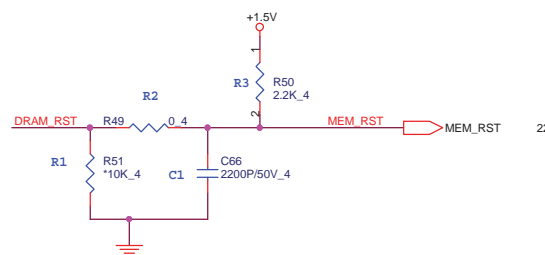


	M9x-S2/S3	Park-S3
MEM_CALRN0 (J25)	NC	240R
MEM_CALRP0 (K25)	NC	240R
MEM_CALRP1 (J8)	240R	150R
TESTEN2#2 (K7)	NC	0R
R1	NC	10K
R2	0R	51R
R3	2.2K	NC
C1	2.2nF	68pF

240R:CS12402FB03
150R:CS11502FB21

0R:CS00002JB38
680R:CS16802JB27

2.2nF:CH22206KB16
68pF:CH06806JB01



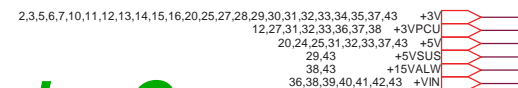
for Park-S3:Use only
for M9x-S3: no support



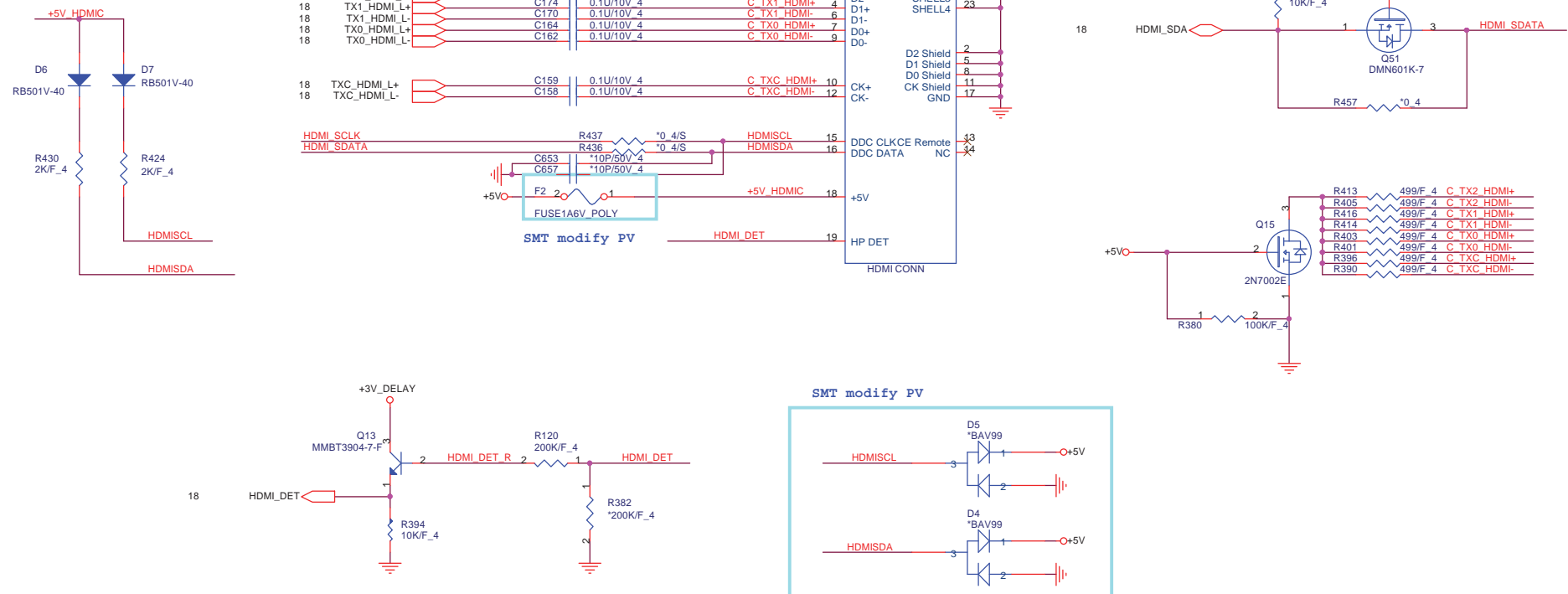
PROJECT : SX7
Quanta Computer Inc.

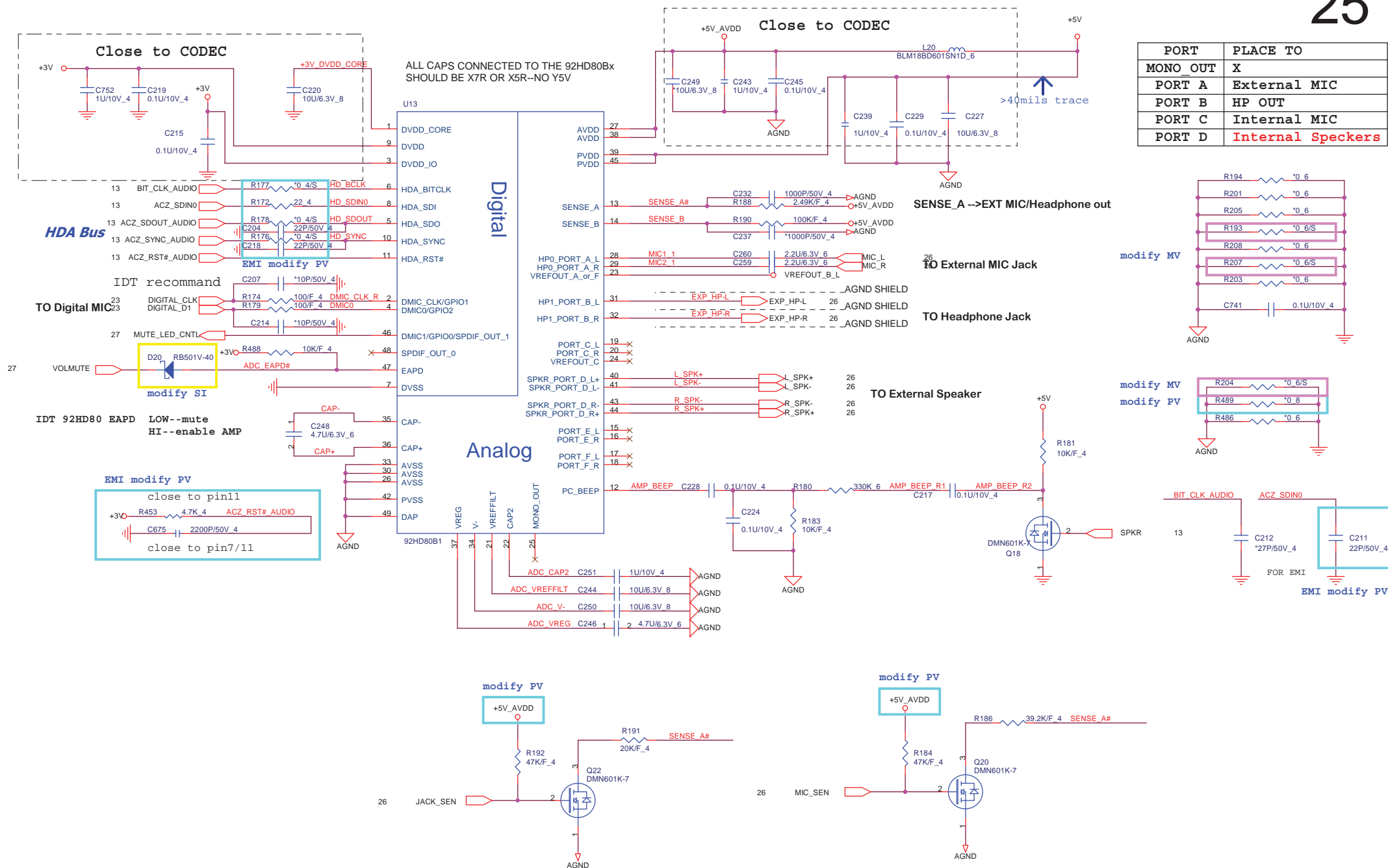
Size	Document Number	Rev
Custom	Park_MEM_Interface	3A
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2.13 LAN_CLKREQ#

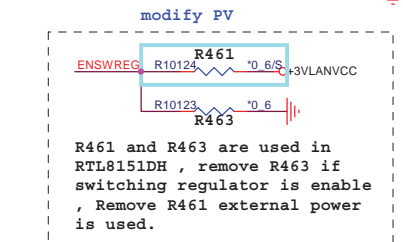
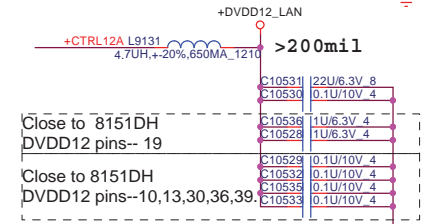
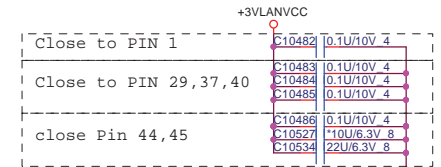
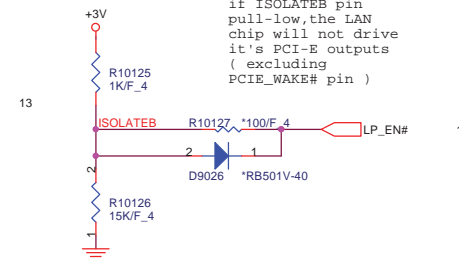
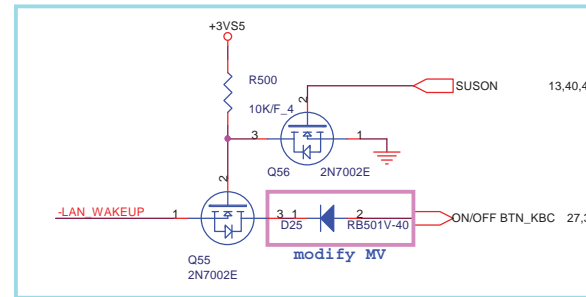
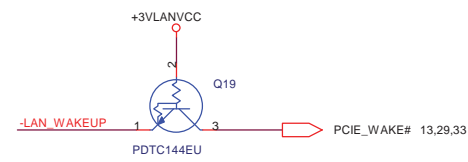
+3VLANVCC

R170 10K/F 4

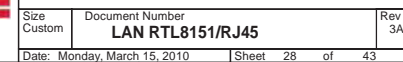
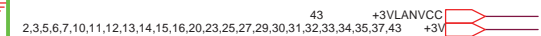
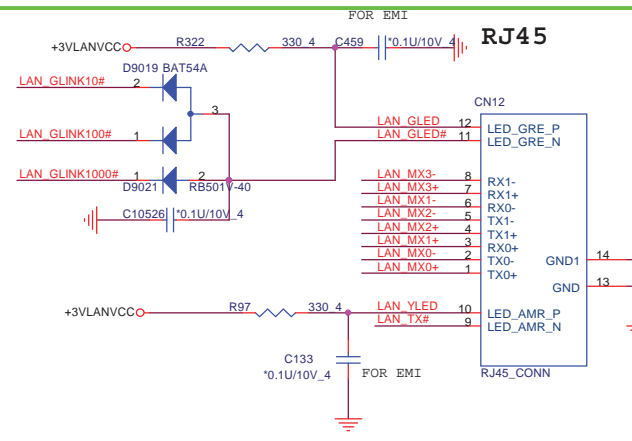
Q17 DMN601-K-7

LAN_REQ#

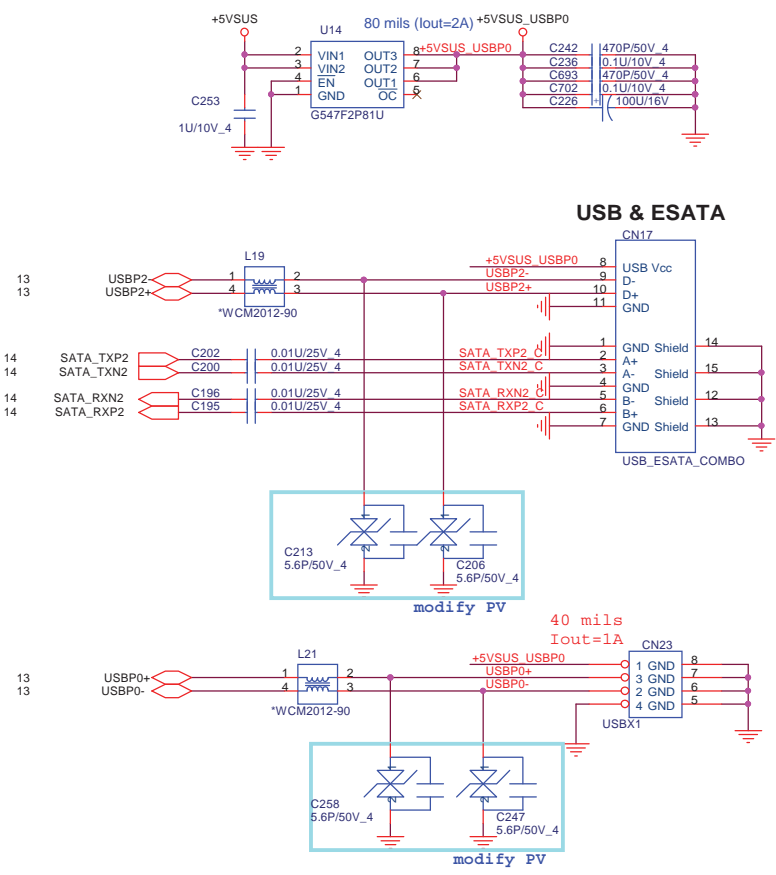
R161 0.4



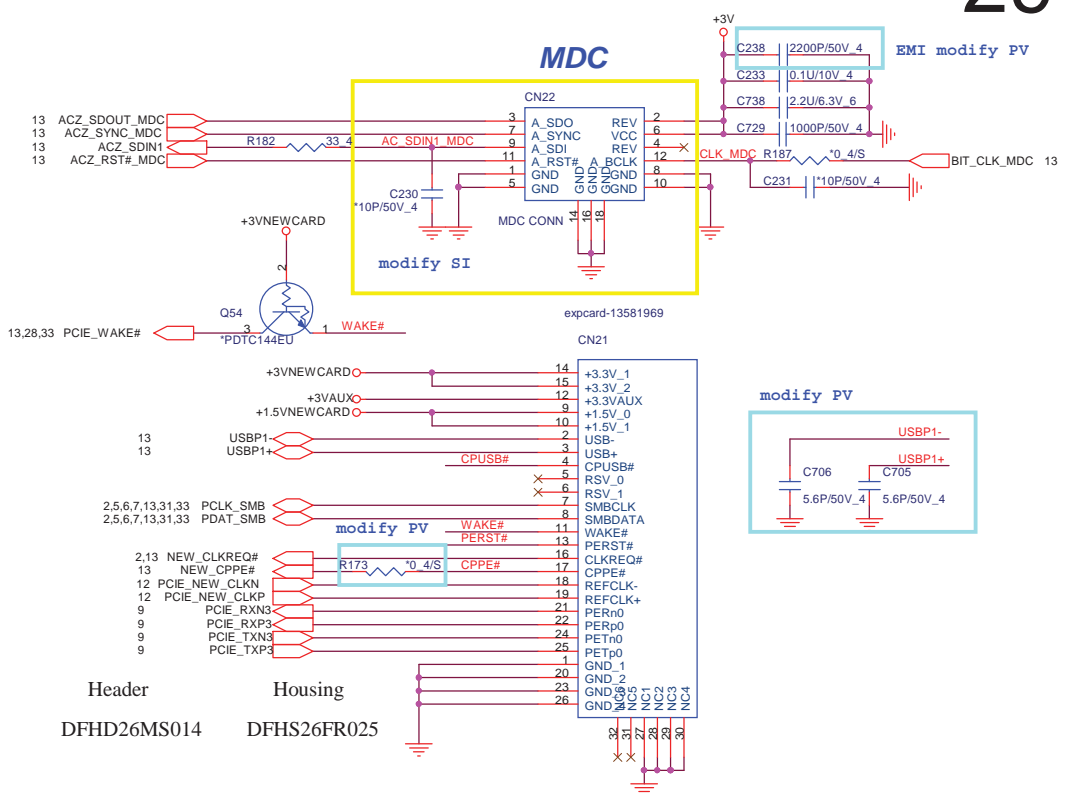
FOR EMI



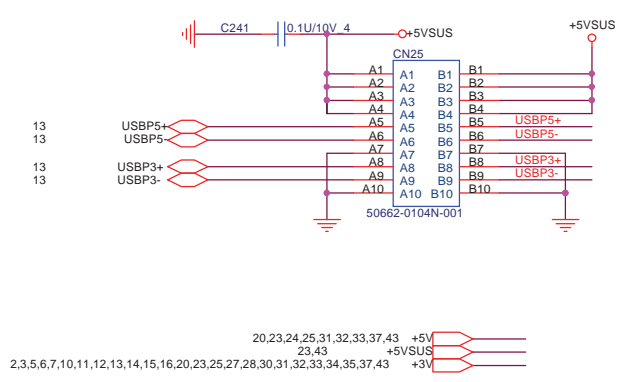
LEFT SIDE USBX1 and E-SATA/USB COMBO



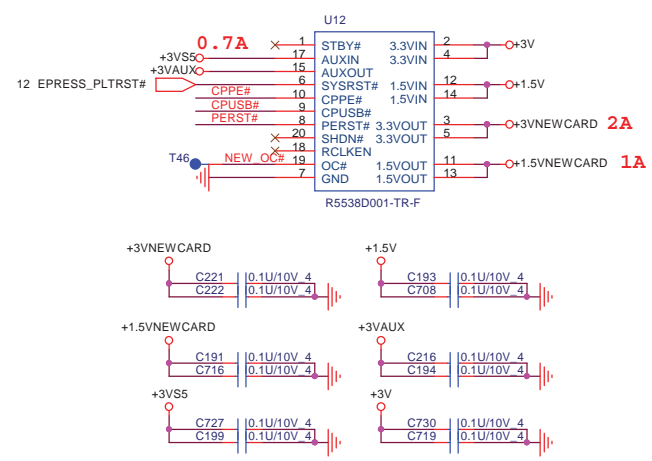
Modem CONN



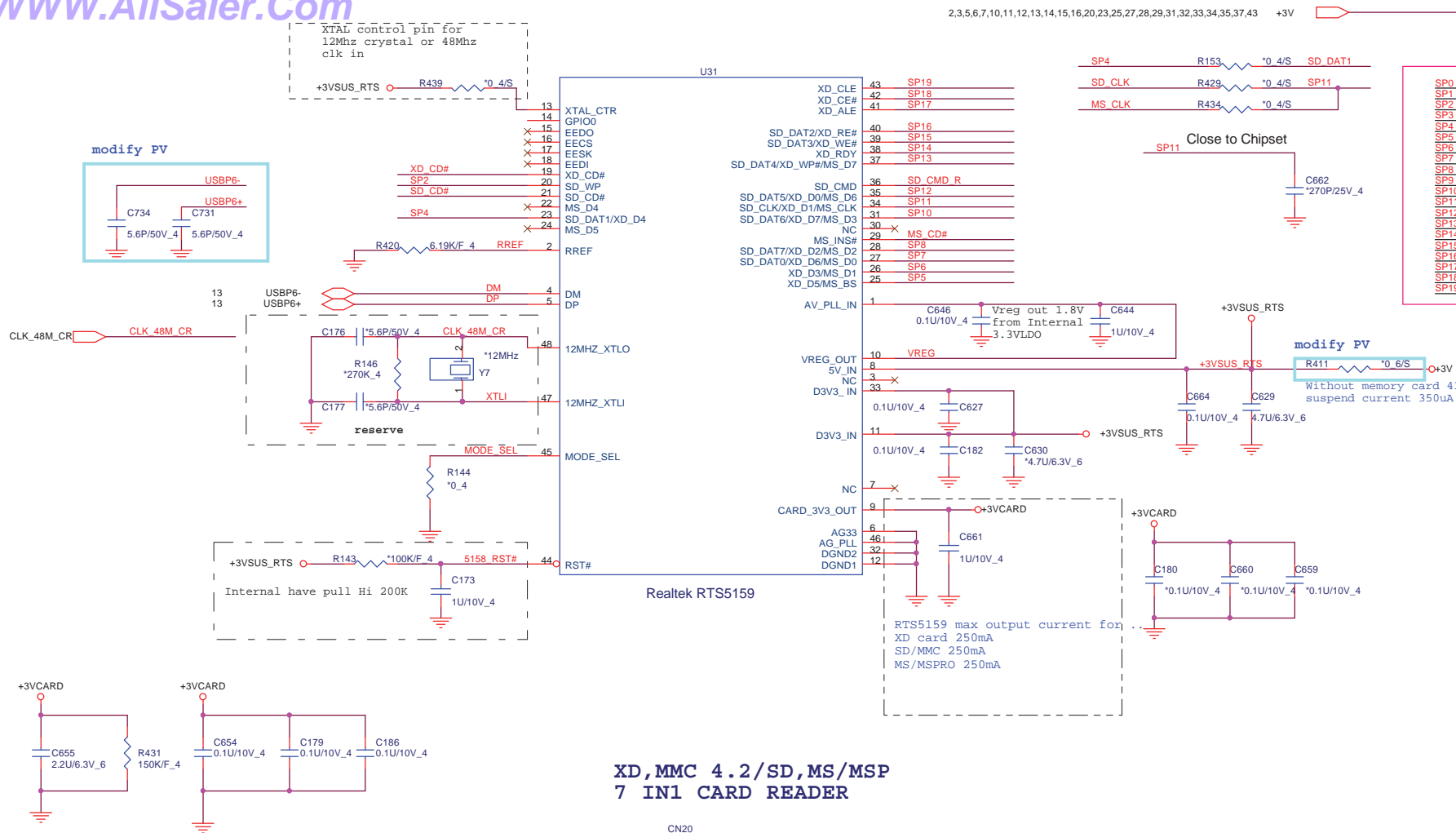
RIGHT SIDE USBX2



NEWCARD (PCIEXPRESS*1 + USB*1)

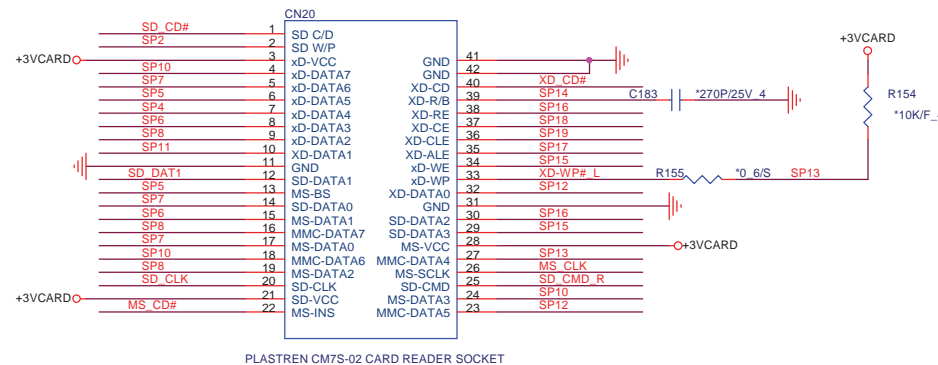


Note:



SD/MMC 4.2		MS	XD
SP0			
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7/MMC_DAT7	MS_D2	XD_D2
SP9			
SP10	SD_DAT6/MMC_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5/MMC_DAT5		XD_D0
SP13	SD_DAT4/MMC_DAT4		XD_WP#
SP14			XD_RB#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

XD,MMC 4.2/SD,MS/MSP
7 IN1 CARD READER



PLASTREN CM7S-02 CARD READER SOCKET



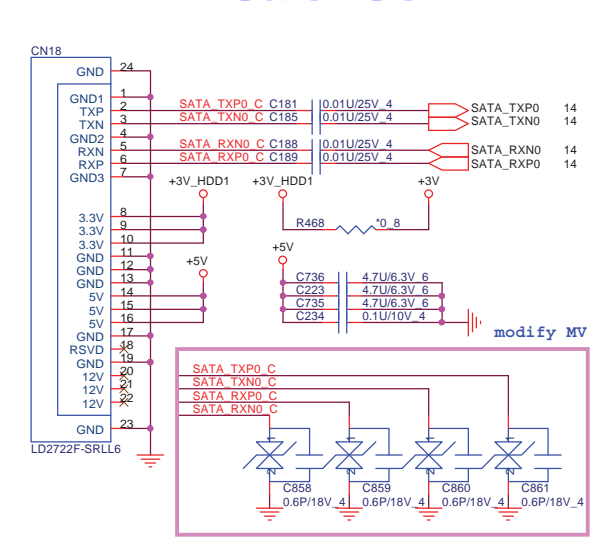
PROJECT : SX7
Quanta Computer Inc.

Size Custom	Document Number RTS5159 & CR SOCKET
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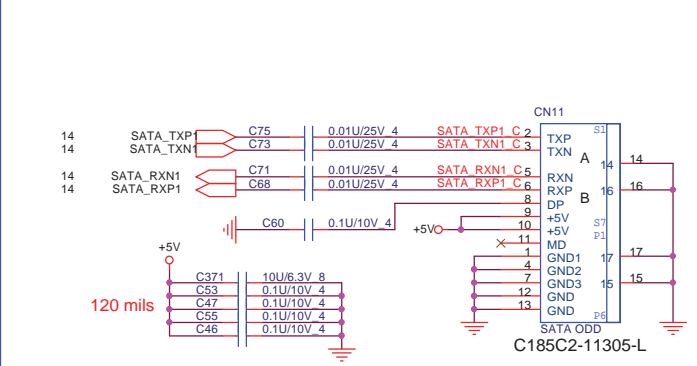
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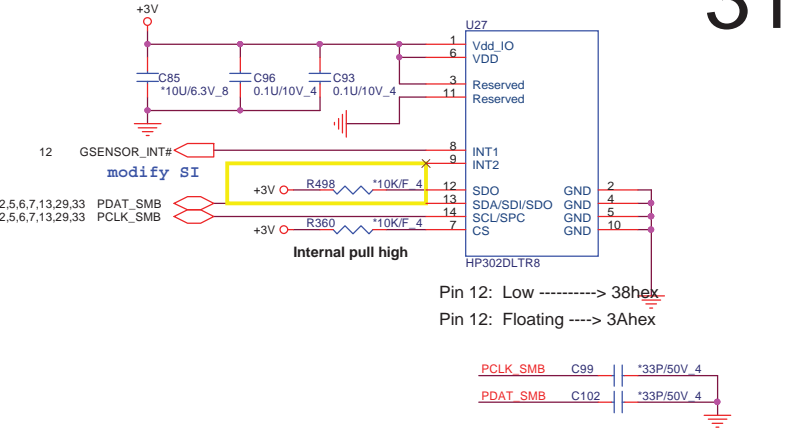
SATA HDD CONNECTOR



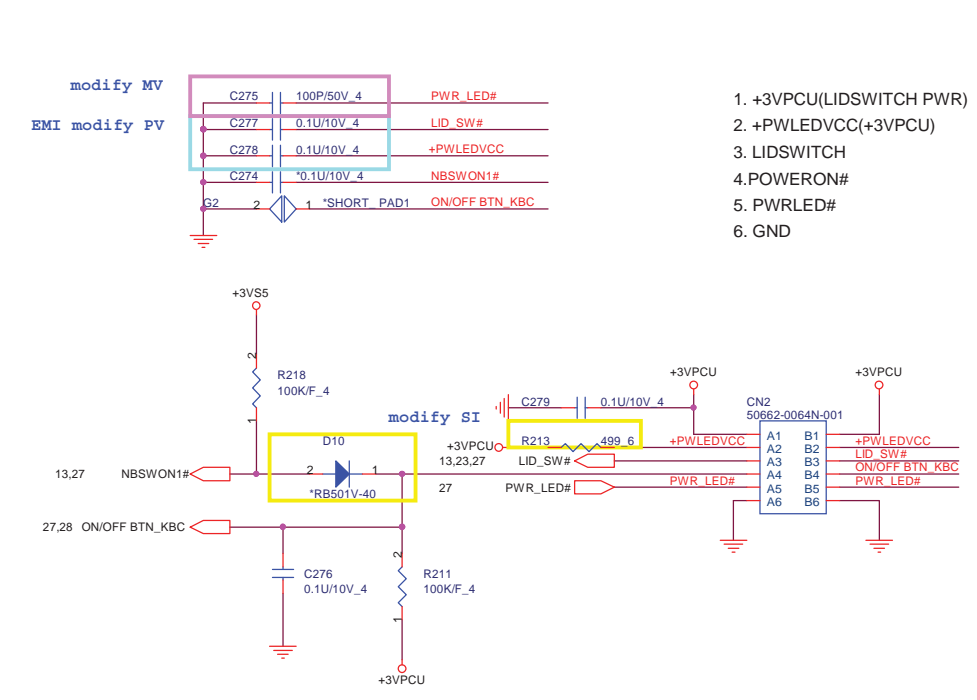
SATA CD-ROM



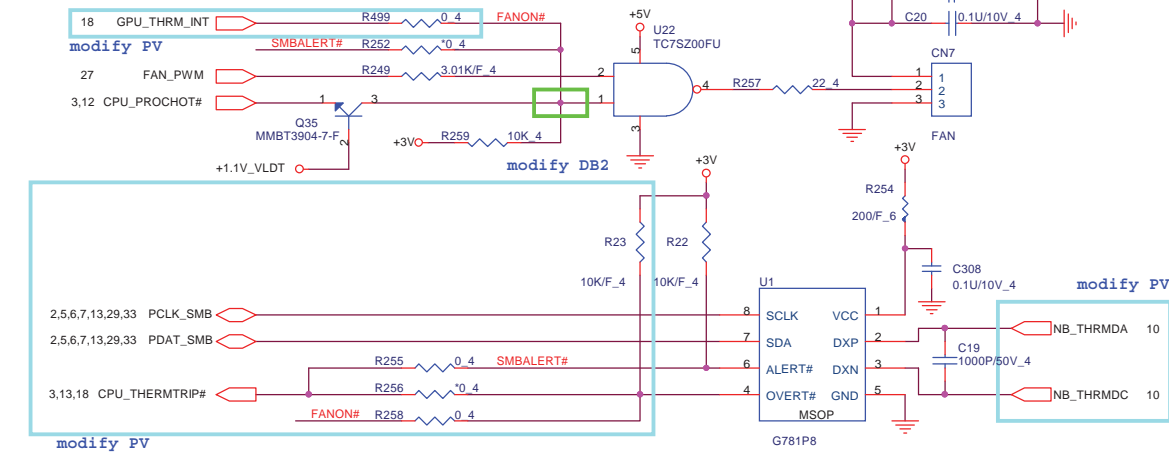
Accelerometer Sensor



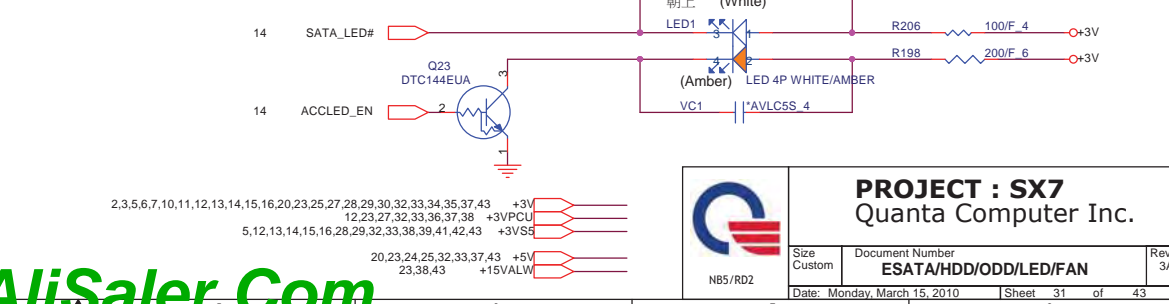
POWER BOTTON CONNECT

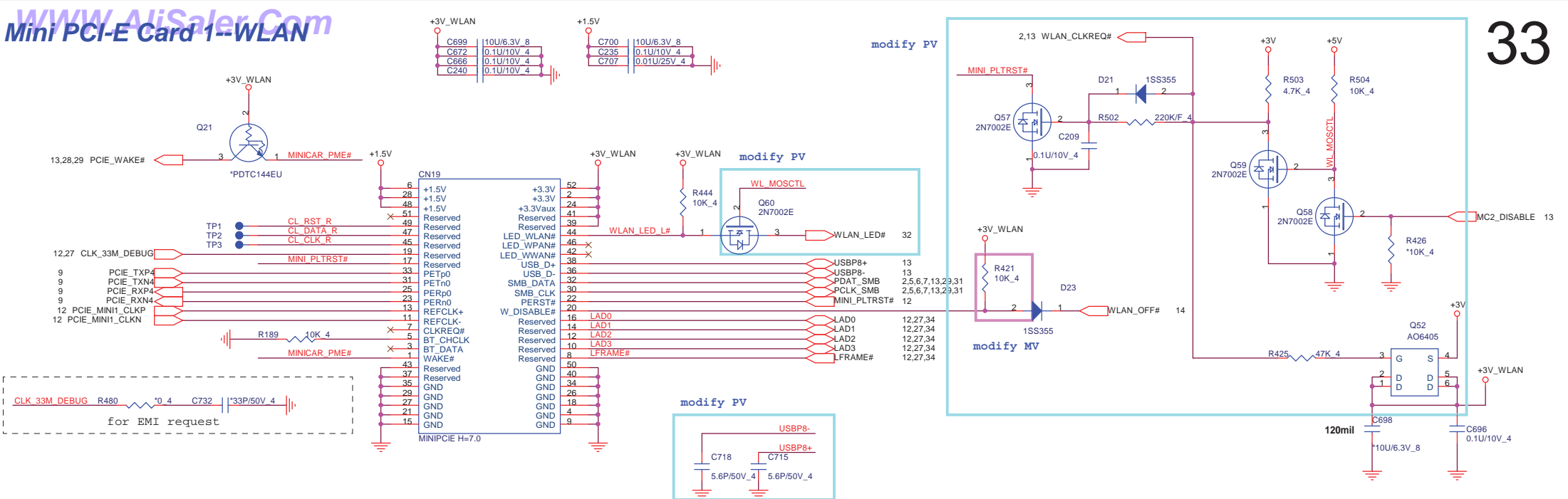


CPU FAN & THERMAL

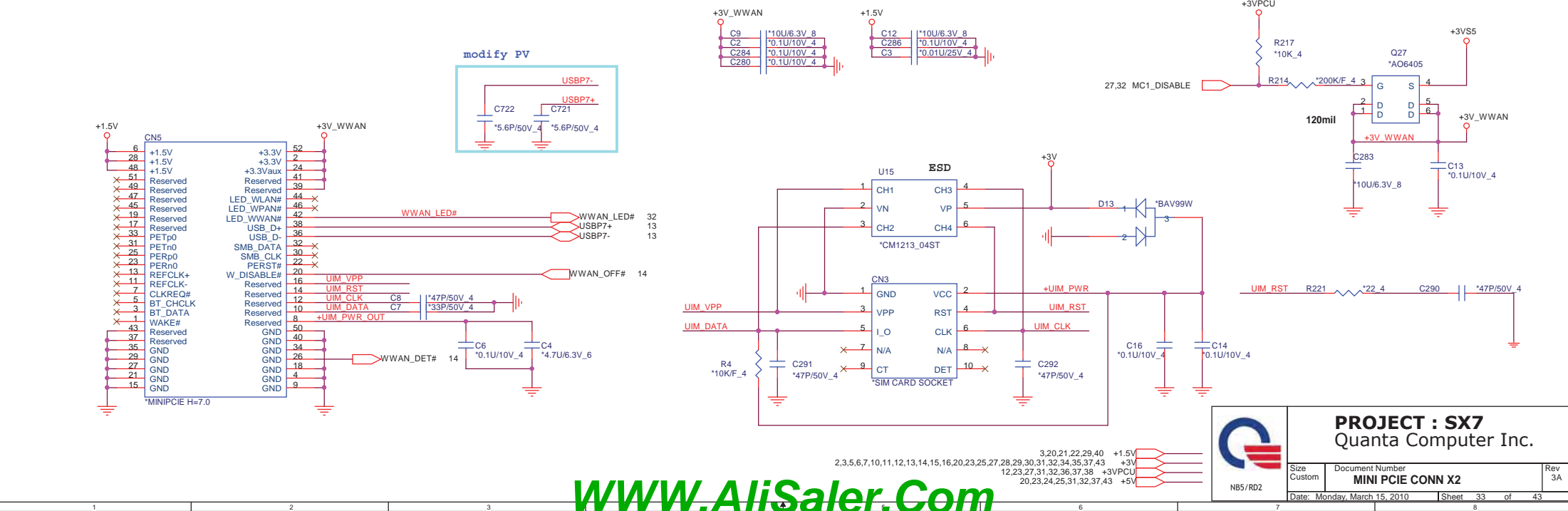


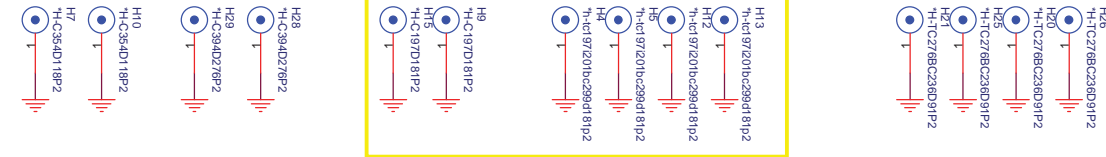
LED



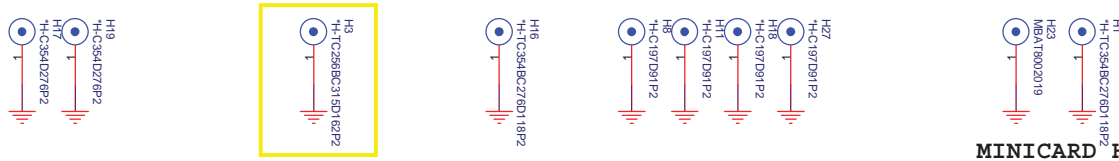


Mini PCI-E Card 2 --WWAN





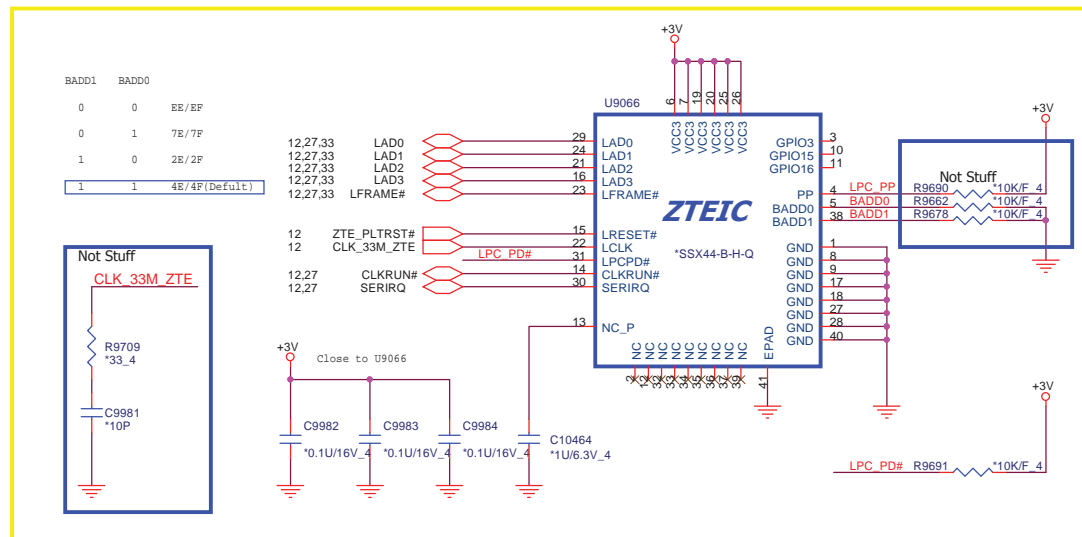
modify SI
VGA HOLE CPU HOLE

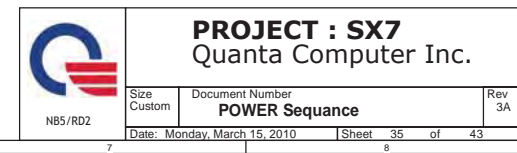


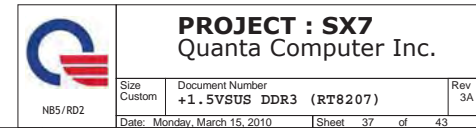
MINICARD HOLE

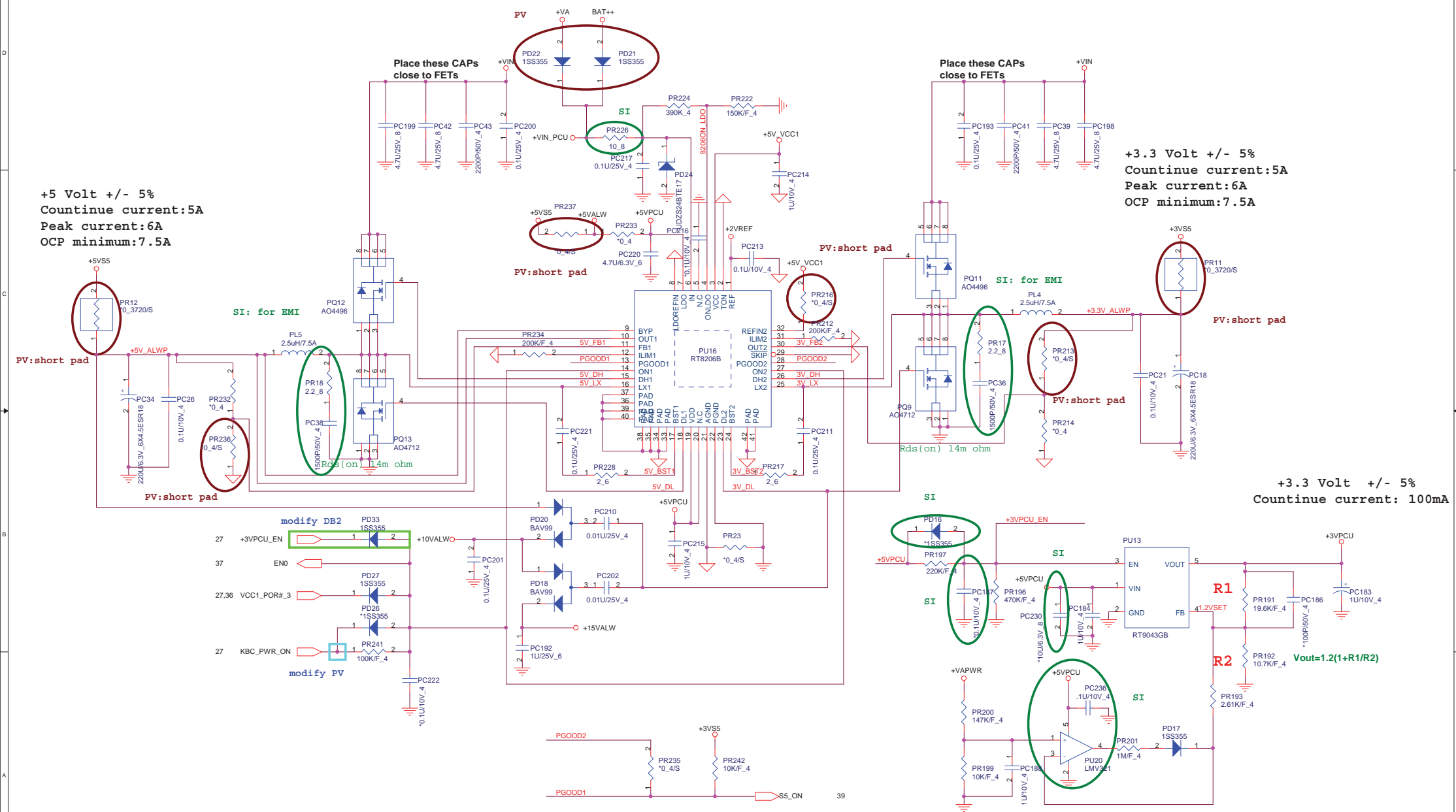
MDC HOLE

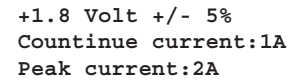
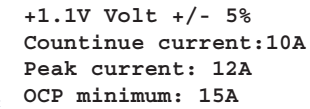
modify SI

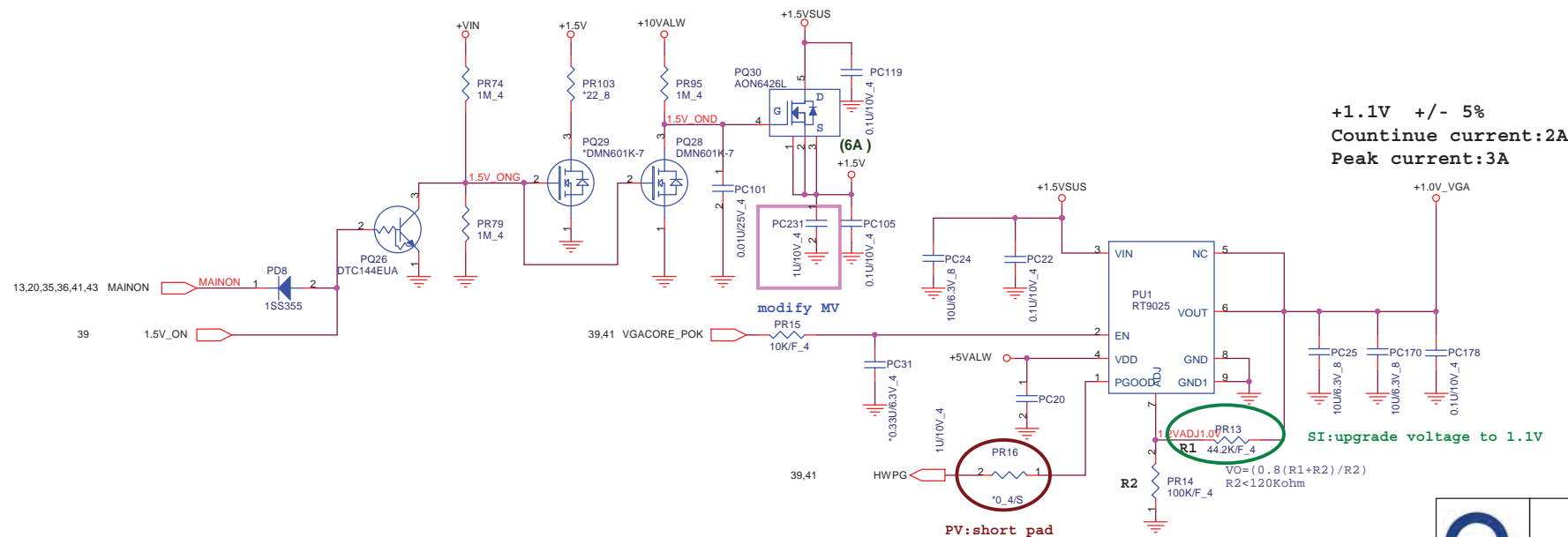
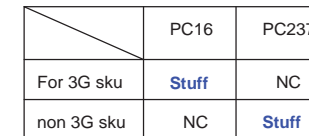






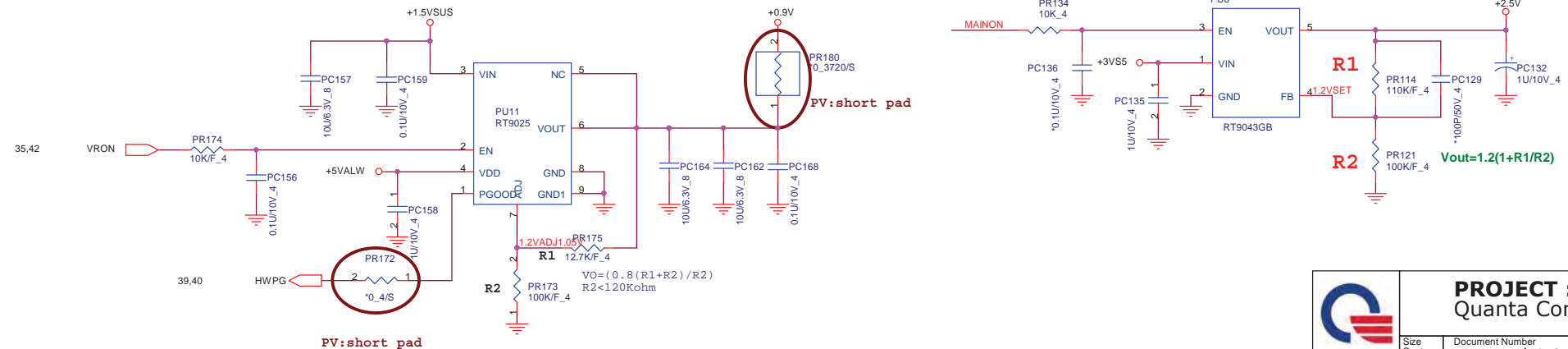
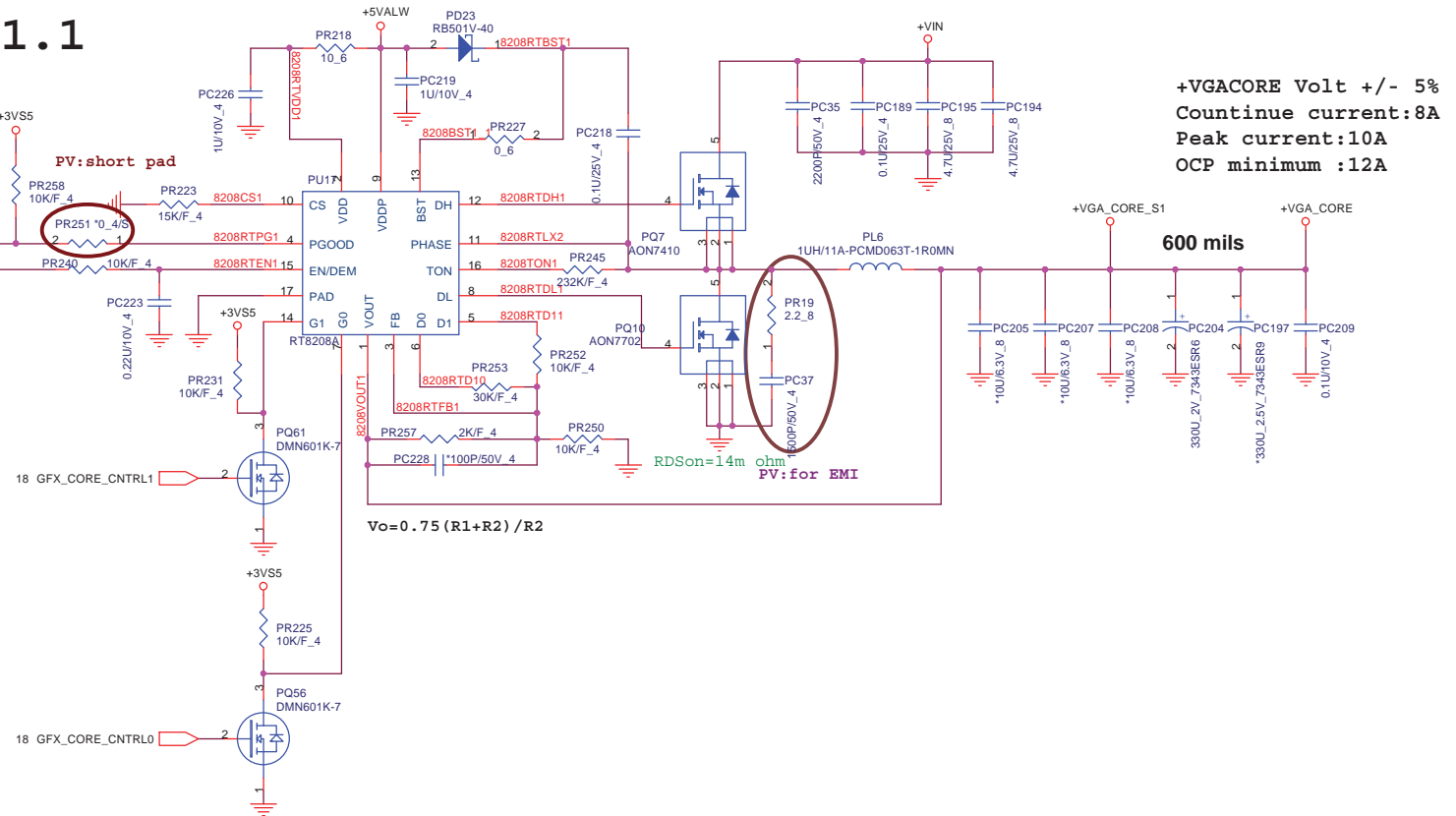






VGA Core & VCC1.1

PWRCNTL1	PWRCNTL0	V-CORE
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V



SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

